(19) World Intellectual Property Organization

International Bureau



I RODIS TIMBURI II BURIN KURI DOMI BERK DIRI KURI KURI KURI KODO KARD IKAD IKAD IKAD IKAD BERKURI DIRI KODI KODI KODI

(43) International Publication Date 18 March 2004 (18.03.2004)

PCT

(10) International Publication Number WO 2004/023312 A1

(51) International Patent Classification⁷: 12/06

G06F 12/08,

(21) International Application Number:

PCT/SG2002/000176

- (22) International Filing Date: 5 August 2002 (05.08.2002)
- (25) Filing Language:

English

(26) Publication Language:

English

- (71) Applicant (for all designated States except US): IN-FINEON TECHNOLGIES AG [DE/DE]; St.-Martin-Strasse 53, 81669 München (DE).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): KAMIKO, Taro [JP/SG]; Block 130 Bishan Street 12 #06-249, Singapore 570130 (SG). PANDEY, Pramod [IN/SG]; Block 226 Pasir Ris Street 21 #11-72, Singapore 510226 (SG).

- (74) Agents: WATKIN, Timothy, Lawrence, Harvey et al.; Lloyd Wise, Tanjong Pagar, P.O. Box 636, Singapore 910816 (SG).
- (81) Designated States (national): CN, IN, US, ZW.
- (84) Designated States (regional): European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR).

Declaration under Rule 4.17:

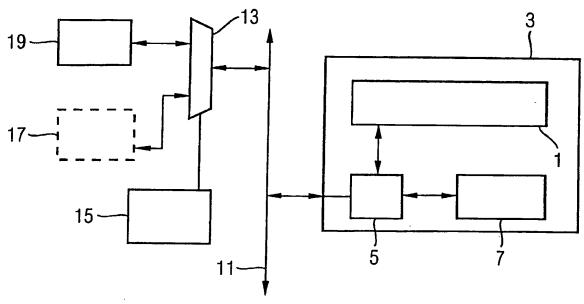
of inventorship (Rule 4.17(iv)) for US only

Published:

with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHODS FOR OPERATING A CPU HAVING AN INTERNAL DATA CACHE



(57) Abstract:—A CPU 3 having a processor 1 and an internal data cache 7 IS operated in combination with a dummy interface 13 which simulates the existence of an external memory 17 having the same address space as the cache memory 7 but which does not store data written to it. In this way, a conventional CPU can be operated without read/write access to an external memory in respect of at least part of its memory address space, and therefore with a higher performance resulting from faster memory access and reduced external memory requirements. The CPU 3 may be one of a set of CPU chips 20, 21 in a data processing system, one or more of those chips 20 optionally having read/write access to an external memory 23.